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*Designing with Xilinx® FPGAs: Using Vivado*

This training content offers introductory training on the Vivado® Design Suite and demonstrates the FPGA design flow for those uninitiated to FPGA design. The courses provide experience with: Creating a Vivado Design Suite project with source files

*Xilinx Customer Learning Center*

UG893 (v2020.1) June 24, 2020 www.xilinx.com Using the Vivado IDE 7. Send Feedback. Designing FPGAs Using the Vivado Design Suite 1. Designing FPGAs Using the Vivado Design Suite 2. Designing FPGAs Using the Vivado Design Suite 3. FPGAs Using the Vivado Design Suite 3. Designing FPGAs Using the Vivado Design Suite 4. UG892. www.xilinx.com

*Vivado Design Suite User Guide: Using the Vivado IDE - Xilinx*

Basic FPGA Architecture; Xilinx Tool Flow; Lab 1: Xilinx Tool Flow. An introduction to FPGA design flow. Open a project containing the PicoBlaze 8-bit microcontroller and simulate the design using the ISim HDL simulator provided with the ISE Foundation software. Architecture Wizard and Pins Assignment; Lab 2: Architecture Wizard and Pins Assignment

*FPGA Design Flow using ISE - Xilinx*

Xilinx has acquired the assets of FPGA compiler developer Falcon Computing Solutions in the US. Falcon's high-level synthesis (HLS) compiler optimisation technology will make adaptive computing more accessible to software developers as part of the Xilinx Vitis unified software platform with automated hardware-aware optimizations.

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## *Xilinx acquires Falcon Computing FPGA compiler technology*

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Build an effective FPGA design using synchronous design techniques, instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments, set global XDC constraints, and use Vivado Design Suite to build, synthesize, implement, and download a design.

## *Vivado | Designing FPGAs Using the Vivado Design Suite 1*

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Basic Design Analysis in the Vivado IDE - Use the various design analysis features in the Vivado Design Suite. {Lab, Demo} Vivado Design Rule Checks - Run a DRC report on the elaborated design to detect design issues early in the flow.

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